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TDM Switch

(iPECS eMG100HW-TRA-02-001)

30 Aug, 2019

Ericsson-LG Enterprise

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REVISION HISTORY

ISSUE	DATE	DESCRIPTION OF CHANGES
0.1	30-Aug-19	Migration from iPECS eMG80HW-TRA-02-001

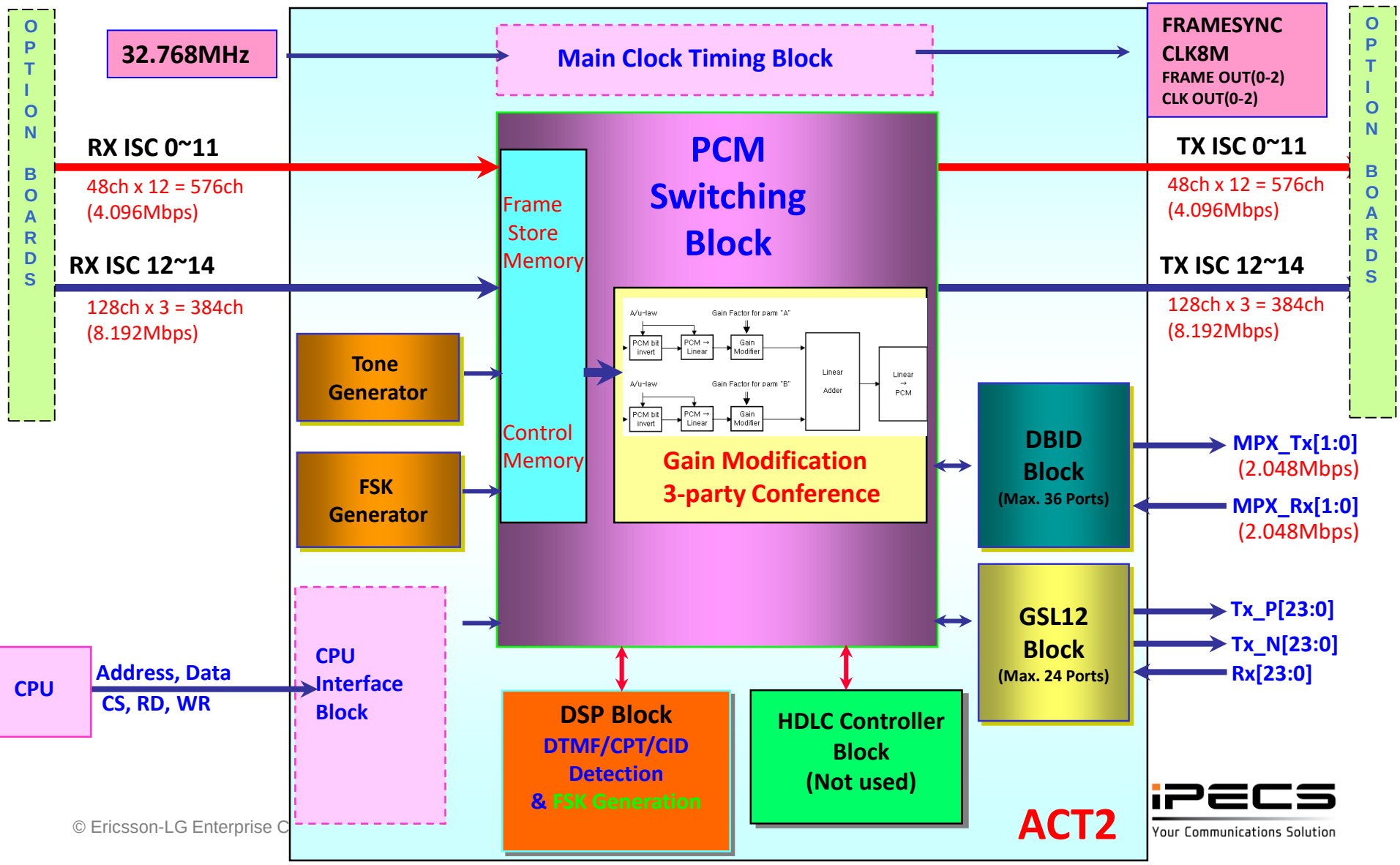
Table of Contents

ACT2

General Description

- PCM switching (max. switching capacity : 12 Highways – 576 ports)
- PCM gain modification (any desired gain value)
- Support channel based programmable A/u-law PCM selection
- Support expansion system highways to increase switching capacity.
- Tone generation (max. 64 tones)
- PCM conference (192 summation locations)
- DBID block has 36 ports interface circuit (MPX mode operation)
- Two GSL12 blocks to support 24 ports digital terminal interface circuit
- Internal 100MHz Zaram DSP (for 32 chs DTMF/CPT/CID)
- Detection and Generation) and Program/Data Memory

Block Diagram



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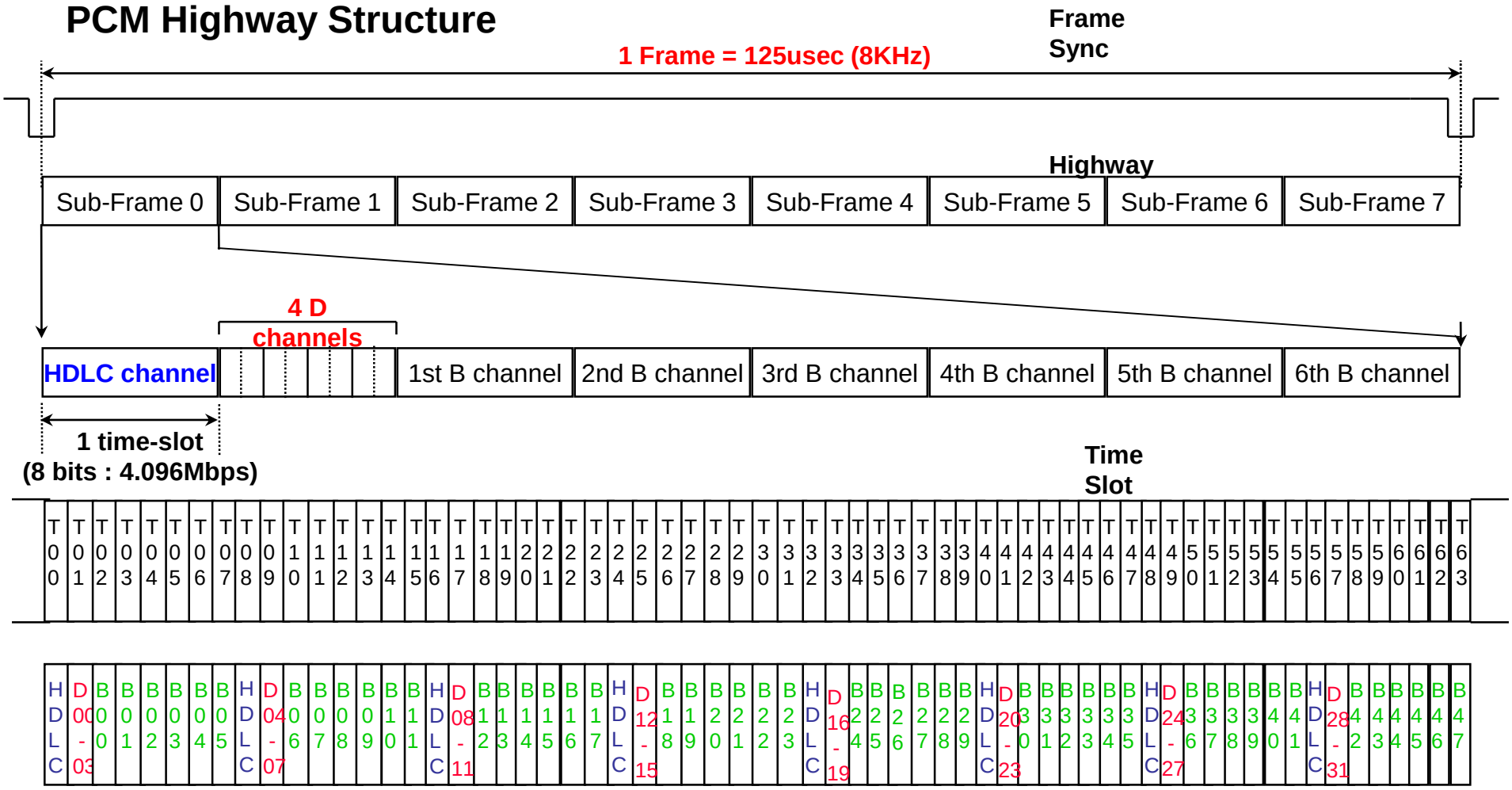
PCM Highway Structure



- 1 Frame of 1 highway contains :

1 HDLC channel (data speed = 8 KHz x 8 bits x 8 Sub-Frame = 512 Kbps)
48 B channels (1B ch, data speed = 8 KHz x 8 bits = 64Kbps)
32 D channels (1D ch, data speed = 8 KHz x 2 bits = 16 Kbps)

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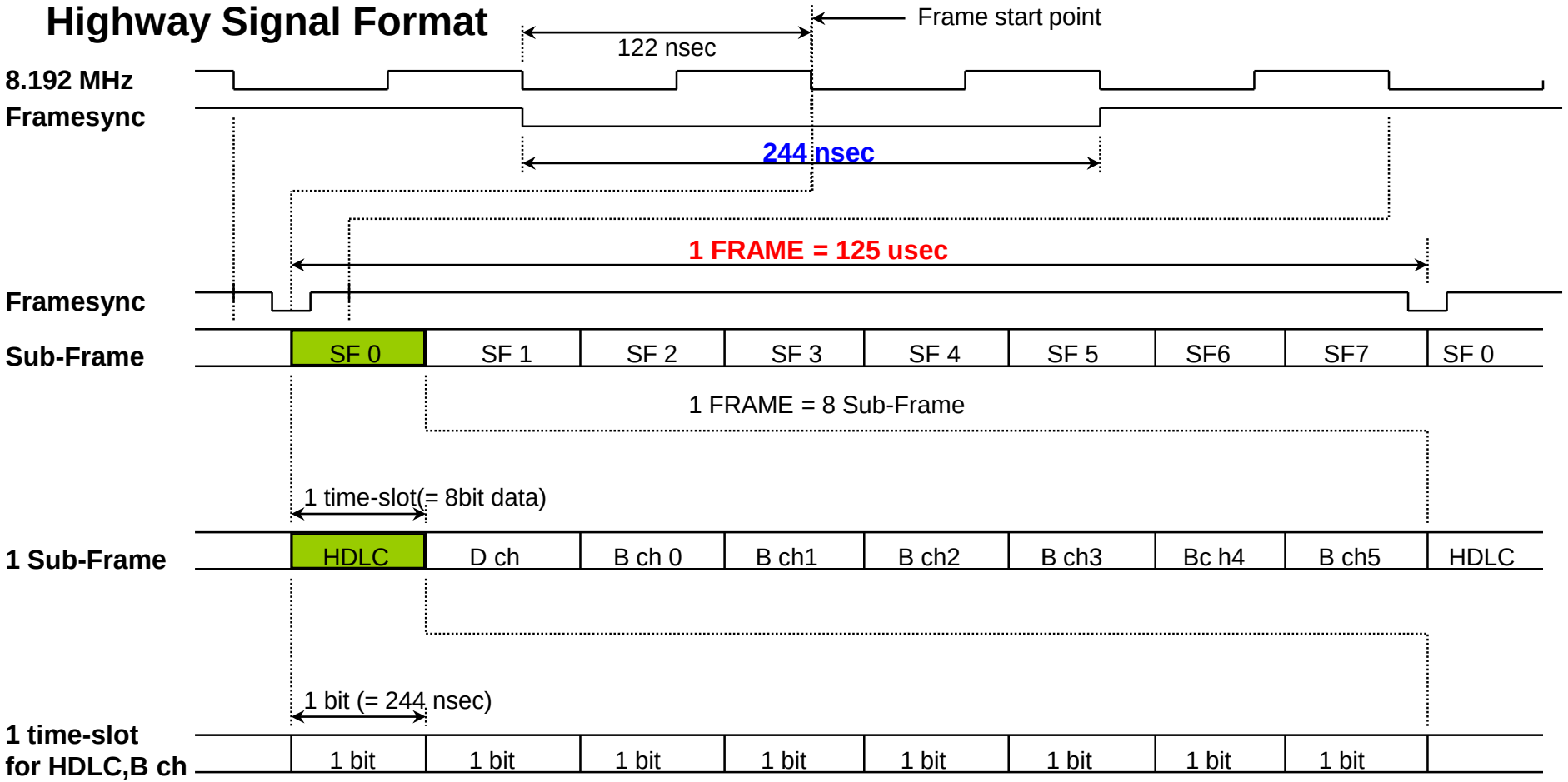
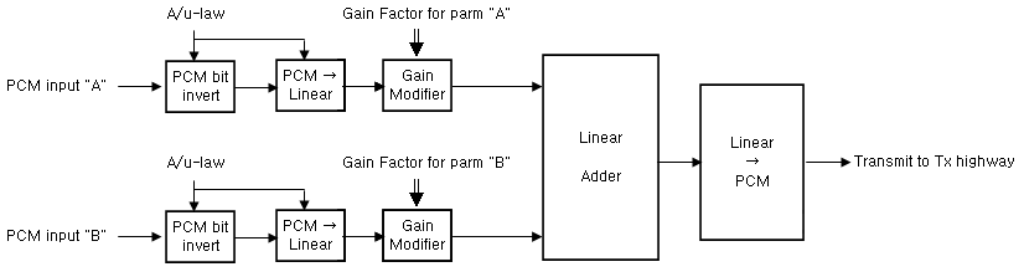
Highway Signal Format



- DATA transfer rate on highway = 4.096 Mbps
- 1 Frame of 1 highway contains
  - -. 1 HDLC channel (8 HDLC time-slot) : 8 time-slot x 8 bit = 64 bit x 8KHz => 512 Kbps x 1ch
  - -. 48 B channel time-slot : 1 time-slot x 8 bit = 8 bit x 8KHz => 64 Kbps x 48ch
  - -. 32 D channel time-slot : 1 time-slot x 2 bit = 2 bit x 8KHz => 16 Kbps x 32ch

ACT2

PCM Switching & Gain Factor



- Supports channel based Programmable A/u-law PCM Selection
- No limitation of 3 party conference
- Supports PCM Conference up to Max. 13 party conference
- Each step changes 0.5dB in normal volume range.

For more detailed volume step, Refer to the right side table.

Gain Step	Level (Gain-dB)	Changing per Step	S/W Gain Step	Level (Gain-dB)	Changing per Step
0	-80.0	Almost Silence	32	0.0	0.5 dB / Step
1	-42.0	6.0 dB / Step	33	0.5	
2	-36.0		34	1.0	
3	-30.0		35	1.5	
4	-24.0	3.0 dB / Step	36	2.0	
5	-21.0		37	2.5	
6	-18.0		38	3.0	
7	-15.0	1.0 dB / Step	39	3.5	
8	-14.0		40	4.0	
9	-13.0		41	4.5	
10	-12.0		42	5.0	
11	-11.0		43	5.5	
12	-10.0	0.5 dB / Step	44	6.0	
13	-9.5		45	6.5	
14	-9.0		46	7.0	
15	-8.5		47	7.5	
16	-8.0		48	8.0	
17	-7.5		49	8.5	
18	-7.0		50	9.0	
19	-6.5		51	9.5	
20	-6.0		52	10.0	
21	-5.5		53	11.0	1.0 dB / Step
22	-5.0		54	12.0	
23	-4.5		55	13.0	
24	-4.0		56	14.0	
25	-3.5		57	15.0	
26	-3.0		58	16.0	
27	-2.5		58	17.0	
28	-2.0		60	18.0	
29	-1.5		61	u law => A law	
30	-1.0		62	A law => u law	
31	-0.5		63	Not used for Voice	

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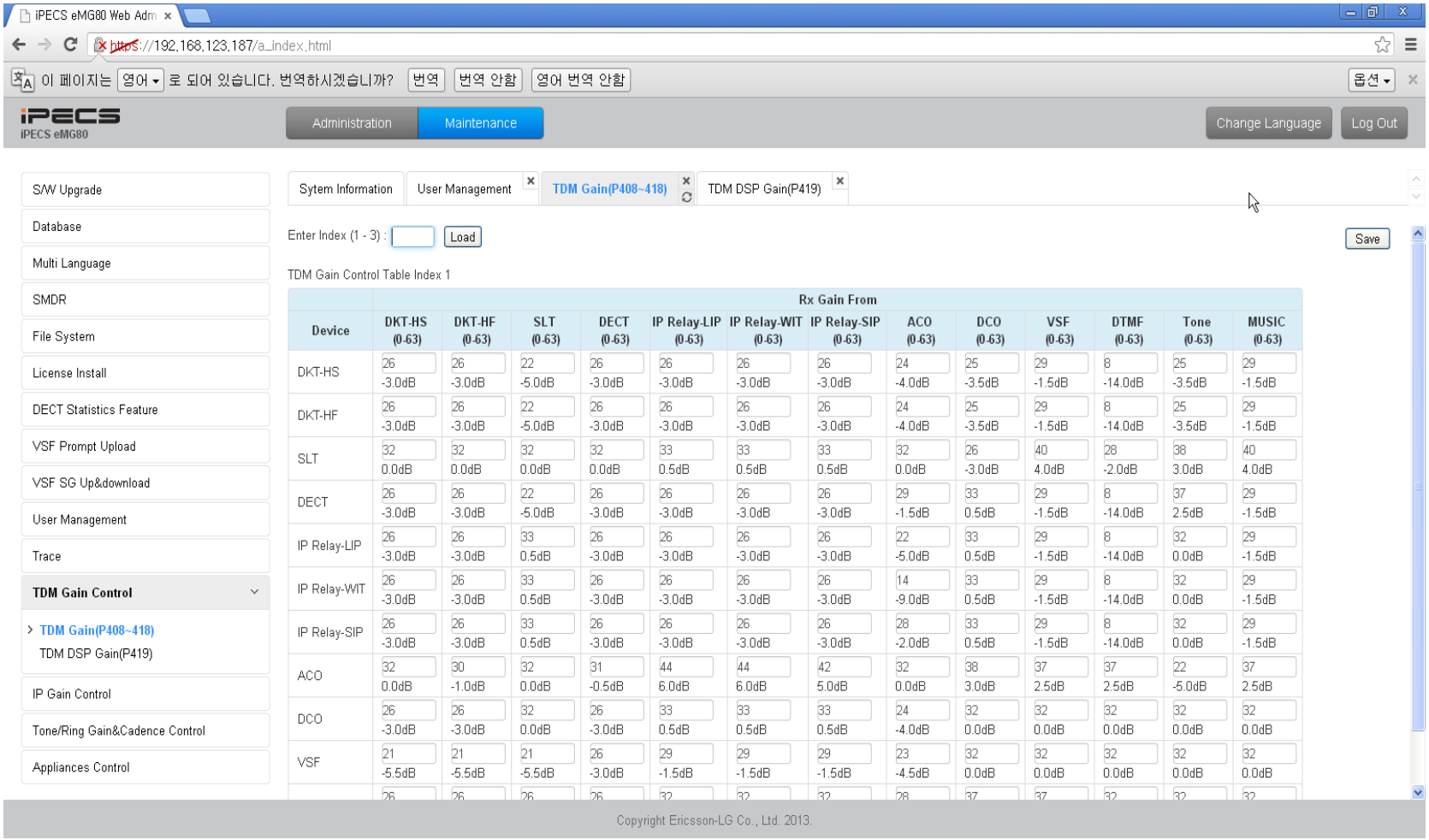
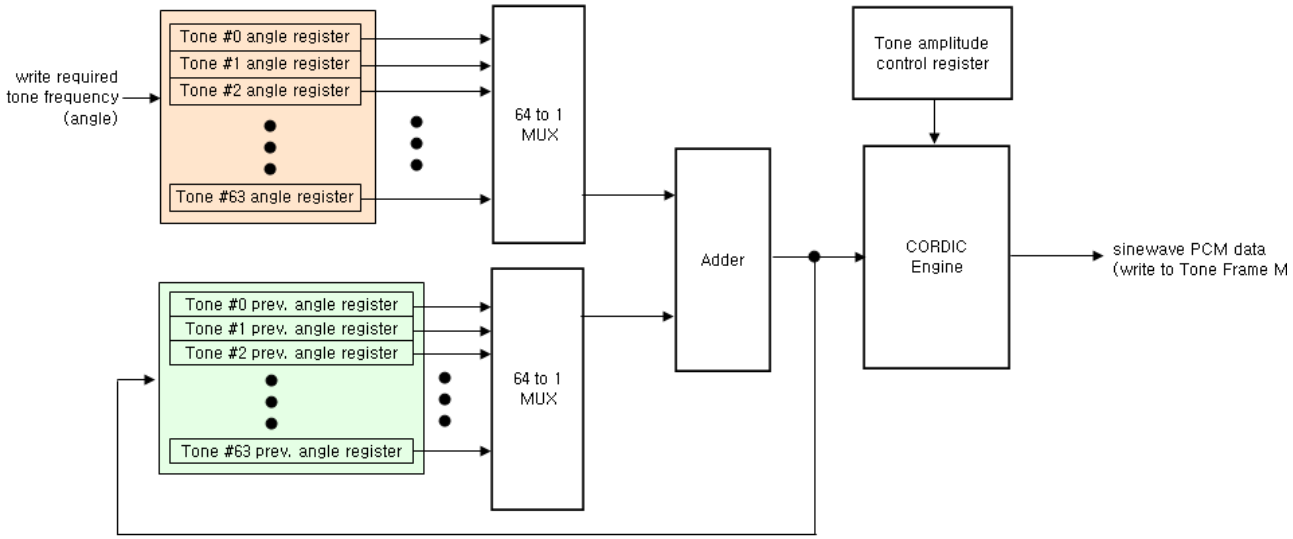
Gain Control



TDM Gain is applied to TDM device

Tone Generator Block



Target tone freq. (Hz)	Angle value in decimal (Tone freq. x 8.192)	Angle value in hexadecimal (Tone freq. x 8.192)
697	5710	0x164E
770	6308	0x18A4
852	6980	0x1B44
941	7709	0x1E1D
1209	9904	0x26B0
1336	10945	0x2AC1
1477	12100	0x2F44
1633	13378	0x3442
350	2867	0x0B33
400	3277	0x0CCD
425	3482	0x0D9A
440	3604	0x0E14
450	3686	0x0E66
480	3932	0x0F5C
525	4301	0x10CD
620	5079	0x13D7
800	6554	0x199A
820	6717	0x1A3D
890	7291	0x1C7B
910	7455	0x1D1F
950	7782	0x1E66
1000	8192	0x2000
1020	8356	0x20A4
1260	10322	0x2852
1280	10486	0x28F6
1400	11469	0x2CCD
1800	14746	0x399A
2280	18678	0x48F6
2500	20480	0x5000
1300	10650	0x299A
2100	17203	0x4333
1200	9830	0x2666
2200	18022	0x4666
2130	17449	0x4429
2750	22528	0x5800

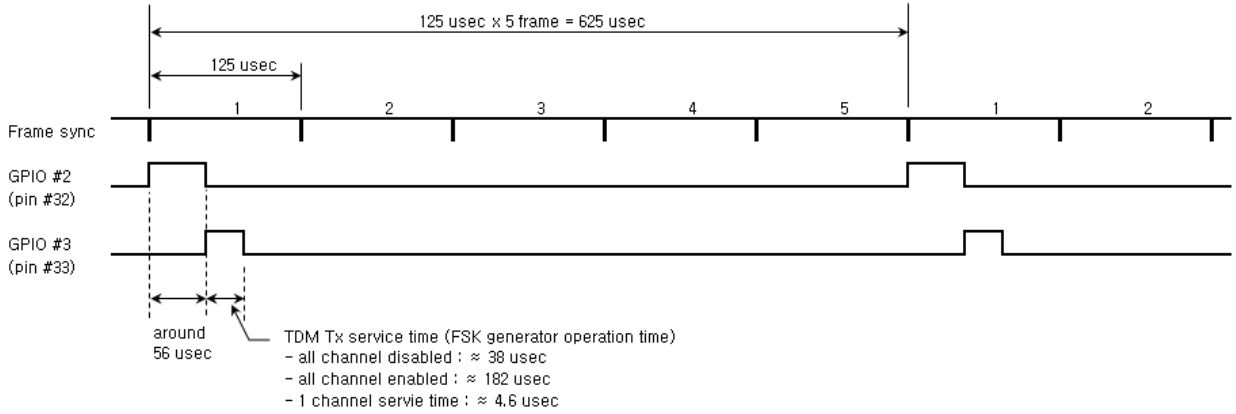
Target Angle = Round [(target freq.) x 125usec x $2^{\text{bit resolution}}$]
= Round [(target freq.) x 125usec x 2^{16}]
= Round [(target freq.) x 8.192]

-. Support Max. 64 Tone channels
-. Any kinds of Tone frequency can be made

FSK Generator Block

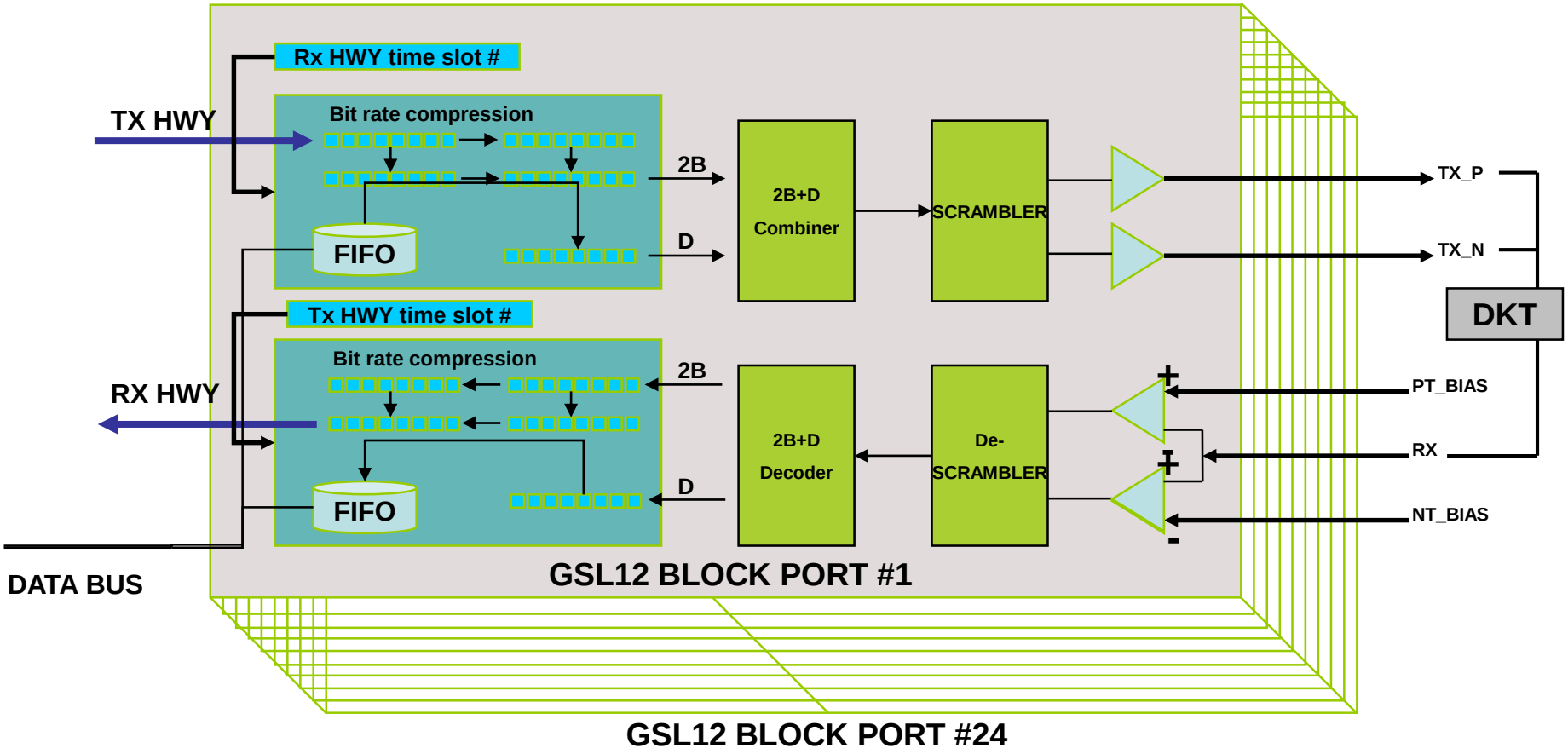
- **Internal DSP S/W supports a FSK signal generation function.**
- **The FSK generator block can support maximum 16 channels without any restrictions.**
- **FSK generator block and other signal detection block are quite independent each other.**
- **FSK transmitting level is fixed around -10dBm.**
  But the real transmitting level can vary by the state of the SLT interface circuit and gain factor of PCM switching circuit.

➢ How to know the DSP S/W is properly running



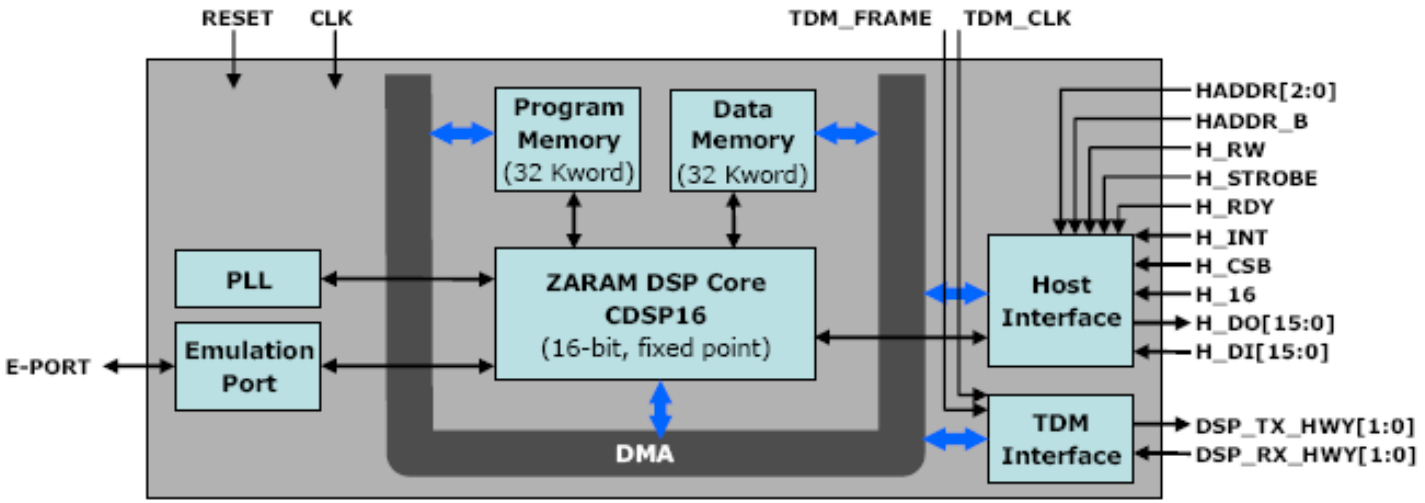
- GPIO #2 (pin #32) : shows TDM Rx interrupt service routine running time
- GPIO #3 (pin #33) : shows TDM Tx interrupt service routine running time
- When you can see above signals with specified time duration, the DSP image is now running properly.

GSL12 Block



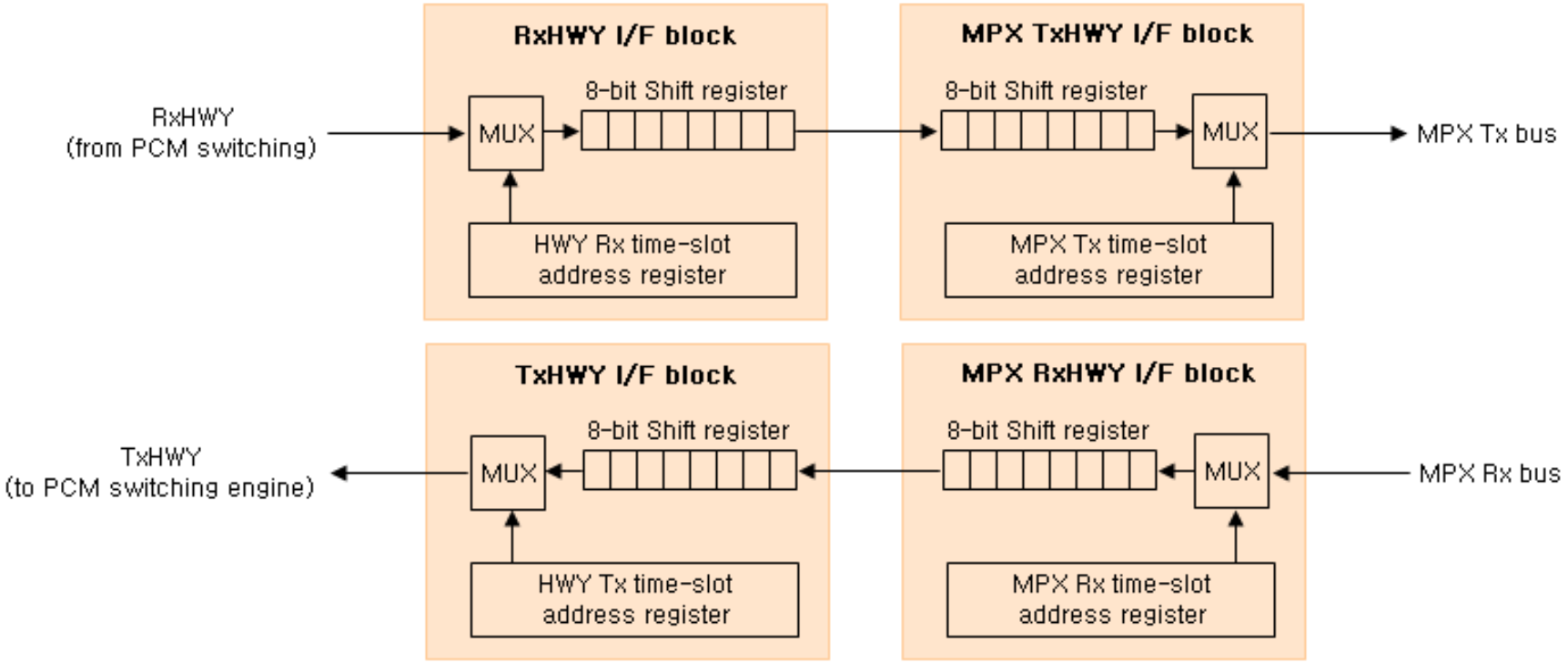
- PT Bias : 1.65V + 135mV = 1.785V
- NT Bias : 1.65V – 135mV = 1.515V
- Support Max. 24 Digital Terminals Interface Circuit

DSP Block



- **Zaram's CDSP16 core** : 16-bit fixed point DSP core can be runs over 100MHz.
- **Program memory** : 32Kword size for running DSP S/W image.
- **Data memory** : 32Kword size for working scratch pad memory.
- **Overlay memory** : 8Kword size and it is located in both program memory space and data memory space. That means, the overlay memory can be used as program memory or data memory.
- **Host interface block** : provides data transfer channel between DSP and external host CPU. External CPU can access both program memory and data memory of DSP by using the host interface block.
- **TDM interface block** : provides PCM data transfer between DSP and external PCM control devices. This block is usually connected with ACT2 DSP_highway itself.
- **DSP Function supports DTMF, CPT and CID Detection and FSK Generation**

DBID Block



- **Support Max. 36 Ports Interface Circuit (MPX Mode Operation)**
- **Support Two MPX bus : MPX Tx/Rx 0, MPX Tx/Rx 1**
- **1 MPX bus consists of 32 time slots , 2.048Mbps**
- **Two MPX bus : Max. 36 Ports interface circuit**